后芮驷(上海)电子有限公司

Horus International Electronics Co., LTD.

承认书

SPECIFICATION FOR APPROVAL

编号:

品名 DESCRIPTION： Camera PMIC

规格 SPEC : HRS-SCT61240Q Series

包装 PACKAGE: Tape & Reel

客户 CUSTOMER：

客户料号 CUSTOMER P/N:

APPROVED BY	
CUSTOMER	HORUS

Quad Channel Power Management IC for Ultra Compact Automotive Camera Module

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Wide Input Voltage Range: 4V-19V
- Synchronous HV Pre-Buck1:
- Up to 1.2A Continuous Output Current
- Auto-adaptive Output Voltage Depends on LDO Output Voltage
- Synchronous LV Post-Buck2:
- Powered by Pre-Buck1
- Up to 0.6A Continuous Output Current
- Fixed Output Voltage of 1.8V
- Synchronous LV Post-Buck3:
- Powered by Pre-Buck1
- Up to 1.2A Continuous Output Current
- Adjustable Output Voltage: 1.1V/1.2V/1.3V/1.5V
- LV Post-LDO:
- Powered by Pre-Buck1
- Up to 0.3A Continuous Output Current
- Adjustable Output Voltage: 2.7V/2.8V/2.9V/3.3V
- Low Noise and High PSRR
- Low Shutdown Current: 1uA
- Fixed 2.2MHz Switching Frequency
- Integrated Frequency Dither for EMI Mitigation
- FCCM Operation
- 60ns Minimum On-time
- 6 Flexible Sequence via External Resistor
- 9 Flexible Output Voltage via External Resistor
- Push-pull Power Good Indicator
- Integrated Hiccup Mode Protection Features:
- Input Over-voltage Protection
- Output Over-voltage Protection
- Output Under-voltage Protection
- Over-current Protection
- Adjustable Under-voltage Lockout
- Thermal Shutdown Protection
- Available in QFN-18L(2.5mm*3.5mm)

APPLICATIONS

- ADAS
- Compact Camera Module
- Cabin Monitor

DESCRIPTION

The SCT61240Q is a highly integrated power management IC (PMIC) optimized for automotive camera system. It integrates three high efficiency synchronous BUCK converters (HVBUCK1, LVBUCK2, LVBUCK3), and a high-PSRR low noise LDO with OV/UV monitoring on all outputs.

VOUT1 is the output of BUCK1, which is powered from VIN (Power Over Coax) and can output 1.2A continuous current with the output voltage set to LDOOUT+300mV/500mV or fixed 3.3V.

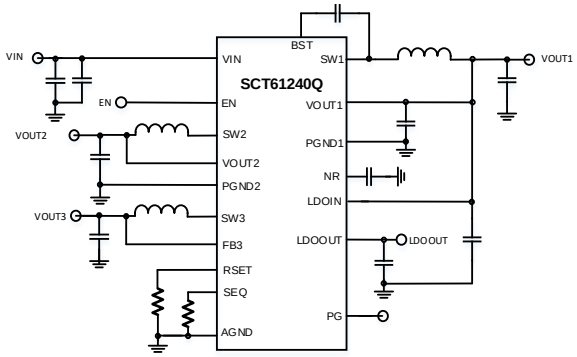
VOUT2 is the output of BUCK2, which is powered from VOUT1 and can output 600mA continuous current with the output voltage fixed to 1.8V.

VOUT3 is the output of BUCK3, which is powered from VOUT1 and can output 1.2A continuous current with the output voltage set to 1.1V/1.2V/1.3V/1.5V through RSET PIN for different sensors.

LDOOUT is the output of LDO, which is powered from VOUT1 (need to connect LDOIN to VOUT1) and can output 300mA continuous current with the output voltage set to 2.7V/2.8V/2.9V/3.3V through RSET PIN for different sensors.

With a compact QFN2.5x3.5 package, the SCT61240Q greatly reduces external components count and PCB space.

TYPICAL APPLICATION



REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 0.8: Customer Sample

Revision 0.81: Update EC

Revision 0.82: Update EC and Device Order Information, add PSRR Curve

DEVICE ORDER INFORMATION

PART NUMBER	VOUT1	PG VOLTAGE	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT61240QFJCR	Fixed 3.3V	3.3V	1240Q	18-Lead 2.5mm×3.5mm FCQFN
SCT61240Q-0000FJCR	LDOOUT+0.3V	1.8V	1240Q	18-Lead 2.5mm×3.5mm FCQFN
SCT61240Q-0001FJCR	LDOOUT+0.5V	1.8V	1240Q	18-Lead 2.5mm×3.5mm FCQFN

ABSOLUTE MAXIMUM RATINGS

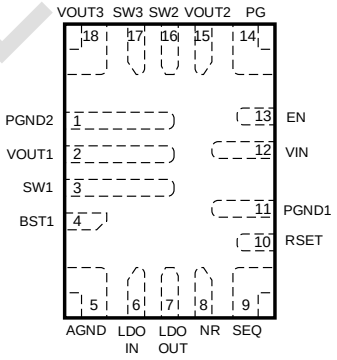
Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	24	V
SW1	-1	24	V
BST-SW1	-0.3	6	V
Others	-0.3	6	V
Junction temperature(2)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 170°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN CONFIGURATION



Top View: 18-Lead FCQFN 2.5mmx3.5mm

PIN FUNCTIONS

NAME	NO.	DESCRIPTION
PGND2	1	Power ground for Buck 2 and Buck 3. Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
VOUT1	2	Feedback for Buck 1 and power source for Buck 2 and Buck 3. Connect VOUT1 pin to the buck 1 output directly. A decoupling capacitor to ground is recommended to be placed close to VOUT1 to minimize switching spikes.
SW1	3	Buck 1 switch node. SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
BST	4	Bootstrap capacitor connection pin for HVBuck1. Connect a 0.1μF ceramic capacitor between this pin and SW1.

PIN FUNCTIONS (continued)

NAME	NO.	DESCRIPTION
AGND	5	Analog ground. AGND is the reference GND for the internal logic and signal circuit. AGND is not internally connected to Power Ground, make sure AGND connected to power ground in PCB.
LDOIN	6	Supply voltage input of LDO. Connect a 2.2μF or larger decouple ceramic capacitor between this pin and ground.
LDOOUT	7	LDO output. Connect a 10μF ceramic decouple capacitor between this pin and ground.
NR	8	Noise reduction. Connect a 0.1μF ceramic capacitor between this pin and ground to reduce LDOOUT noise.
SEQ	9	Power sequence selection. Connect a resistor between this pin and ground to set the power up sequence. See SEQ setting table.
RSET	10	Output voltage selection for all channels. Connect a resistor between this pin and ground to set the output voltage. See RSET setting table.
PGND1	11	Power ground for Buck 1. Should be electrically connected to the system power ground plane with the shortest and lowest-impedance connection possible.
VIN	12	Input supply voltage. A decoupling capacitor to ground is recommended to be placed close to VIN to minimize switching spikes.
EN	13	Chip enable. Set EN high to enable the part. EN pin is also a high voltage PIN which can connect to VIN.
PG	14	Power good indication for all channels. PG output is push-pull, PG at high state indicates all outputs work well.
VOUT2	15	Feedback for Buck 2. Connect VOUT2 pin to the buck 2 output directly.
SW2	16	Buck 2 switch node. SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
SW3	17	Buck 3 switch node. SW is the output of the internal power switch. Connect to an external inductor using a wide PCB trace.
VOUT3	18	Feedback for Buck 3. Connect VOUT3 pin to the buck 3 output directly.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4	19	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per AEC-Q100-002	-1.5	1.5	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	1	kV

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	QFN-18L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	56.6	°C/W
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	46.8	

THERMAL INFORMATION (continued)

PARAMETER	THERMAL METRIC	QFN-18L	UNIT
$R_{\theta JB}$	Junction to board thermal resistance(1)	8.8	°C/W

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT61240Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT61240Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

V_{IN}=10V, T_A=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		4		19	V
V_{IN_UVLO}	Input UVLO Rising Threshold			3.8	4	V
	Hysteresis			200		mV
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		1	10	μA
I_Q	Quiescent current from VIN pin	EN=3V, no load, non-switching		1	2	mA
I_{Q_ACTIVE}(1)	Quiescent current from VIN pin	EN=3V, no load, switching		10		mA
Enable						
V_{EN}	EN rising threshold		1.1	1.2	1.3	V
	EN hysteresis			100		mV
I_{EN}	EN Pin Input Leakage	EN=5V, VIN=0V		0.01	1	μA
Oscillator and Timing						
F_{SW}	Switching Frequency		2	2.2	2.4	MHz
FSS	Spread Spectrum range		4	5	6	%
	Spread Spectrum frequency		4	5	6	kHz
T_{ON_MIN}	Minimum On Time			60		ns
T_{OFF_MIN}	Minimum Off Time			60		ns
T_{SS_BK1}	BUCK1 soft start time	V_{OUT1}=3.1V, from 0 to 100%		400		μs
T_{SS_BK2}	BUCK2 soft start time	V_{OUT2}=1.8V, from 0 to 100%		400		μs
T_{SS_BK3}	BUCK3 soft start time	V_{OUT3}=1.2V, from 0 to 100%		400		μs
T_{SS_LDO}	LDO soft start time	V_{OUT4}=2.8V, C_{NR}=100nF, C_{OUT}=10μF, I_{LOAD}=100mA		100	300	μs
T_{PG_delay}(1)	PG delay	Default setting		3.6		ms
T_{hiccup}	Hiccup time		2	3.6	5.2	ms
BUCK1 (HV BUCK)						
V_{OUT1}	VOUT1 Output Voltage	SCT61240Q		3.3		V
		SCT61240Q-0000		V_{LDO}+0.3		
		SCT61240Q-0001		V_{LDO}+0.5		
V_{OUT1_ACC}	VOUT1 Accuracy		-2		2	%
$R_{DS\_H\_BK1}$	High-side MOSFET on-resistance	V_{BST1}-V_{SW1}=5V		175	350	mΩ
$R_{DS\_L\_BK1}$	Low-side MOSFET on-resistance	VIN>5V		75	150	mΩ
$I_{ILEAK\_HS\_BUCK1}$	SW1 HS Switch Leakage Current			0.01	1	μA
$I_{ILEAK\_LS\_BUCK1}$	SW1 LS Switch Leakage Current			0.01	1	μA
I_{PEAK_BUCK1}	Peak Current Limit		1.6	2	2.4	A
I_{VALLEY_BUCK1}	Valley Current Limit		1.4	1.8		A
$I_{REVERSE\_BUCK1}$	Reverse Current Limit		1			A
I_{ILEAK_VOUT1}	VOUT1 PIN Leakage	VIN=EN=0V		100	150	μA
R_{DIS_BUCK1}	VOUT1 Output Discharge resistance			50		Ohm

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=10V, T_A=-40°C~125°C, typical values are tested under 25°C

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
BUCK2 (LV BUCK)						
V_{IN23}	VIN23 Input Voltage Range		2.7		5	V
V_{OUT2}	VOUT2 Output Voltage			1.8		V
V_{OUT2_ACC}	VOUT2 Accuracy		-2		2	%
$R_{DS\_H\_BK2}$	High-side MOSFET on-resistance	V_{OUT1}=3.1V		155		mΩ
$R_{DS\_L\_BK2}$	Low-side MOSFET on-resistance	VIN>5V		75		mΩ
$I_{ILEAK\_HS\_BUCK2}$	SW2 HS Switch Leakage Current			0.01	1	μA
$I_{ILEAK\_LS\_BUCK2}$	SW2 LS Switch Leakage Current			0.01	1	μA
I_{PEAK_BUCK2}	Peak Current Limit		0.9	1.2	1.65	A
I_{VALLEY_BUCK2}	Valley Current Limit		0.7	1	1.2	A
$I_{REVERSE\_BUCK2}$	Reverse Current Limit			0.7		A
I_{ILEAK_VOUT2}	VOUT2 PIN Leakage			1	10	μA
R_{DIS_BUCK2}	VOUT2 Output Discharge resistance			50		Ohm
BUCK3 (LV BUCK)						
V_{IN23}	VIN23 Input Voltage Range		2.7		5	V
V_{OUT3}	VOUT3 Output Voltage			1.1/ 1.2/ 1.3/ 1.5		V
V_{OUT3_ACC}	VOUT3 Accuracy		-2		2	%
$R_{DS\_H\_BK3}$	High-side MOSFET on-resistance	V_{OUT1}=3.1V		155		mΩ
$R_{DS\_L\_BK3}$	Low-side MOSFET on-resistance	VIN>5V		75		mΩ
$I_{ILEAK\_HS\_BUCK3}$	SW3 HS Switch Leakage Current			0.01	1	μA
$I_{ILEAK\_LS\_BUCK3}$	SW3 LS Switch Leakage Current			0.01	1	μA
I_{PEAK_BUCK3}	Peak Current Limit		1.55	2	2.65	A
I_{VALLEY_BUCK3}	Valley Current Limit			1.7		A
$I_{REVERSE\_BUCK3}$	Reverse Current Limit			0.7		A
I_{ILEAK_VOUT3}	VOUT3 PIN Leakage			1	10	μA
R_{DIS_BUCK3}	VOUT3 Output Discharge resistance			50		Ohm
LDO						
V_{LDOIN}	LDOIN Input Voltage Range		2.7		5	V
V_{LDO}	LDO Output Voltage			2.7/ 2.8/ 2.9/ 3.3		V
V_{LDO_ACC}	LDO Output Voltage Accuracy		-2		2	%
V_{DROP_LDO}	LDO Dropout Voltage	LDOIN=2.9V, setting LDO output =2.8V, ILDO = 300mA		110	200	mV
$L_{DO\_LINE\_REG}$	LDO Line Regulation	LDOOUT set to 2.7V, LDOIN=3V to 5V, ILDO = 100mA		0.02		%/V
$L_{DO\_LOAD\_REG}$	LDO Load Regulation	LDOIN=3.3V, LDOOUT=2.7V, ILDO from 10mA to 300mA.		0.03		%

ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=10V, T_A=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I_{LIM_LDO}	LDO Current Limit	LDOIN=3 V, setting LDOOUT to 2.8V, force LDOOUT=2.5V	350	400	450	mA
$PSRR_{\_LDO}$	LDO PSRR	LDOIN= 3.1V, LDOOUT=2.8V, C(NR)=100nF, COUT=20μF, ILDO = 100mA @ 1kHz		70		dB
		LDOIN= 3.1V, LDOOUT=2.8V, C(NR)=100nF, COUT=20μF, ILDO = 100mA @ 10kHz		56		dB
		LDOIN= 3.1V, LDOOUT=2.8V, C(NR)=100nF, COUT=20μF, ILDO = 100mA @ 100kHz		35		dB
		LDOIN= 3.1V, LDOOUT=2.8V, C(NR)=100nF, COUT=20μF, ILDO = 100mA @ 1MHz		29		dB
		LDOIN= 3.1V, LDOOUT=2.8V, C(NR)=100nF, COUT=20μF, ILDO = 100mA @ 2.2MHz		24		dB
$eN_{\_LDO}$	LDO noise	LDOIN= 3.1V, LDOOUT=2.8V, C(NR)=100nF, COUT=20μF, ILDO = 100mA, From 10Hz to 100kHz		30		μV_{rms}
I_{ILEAK_LDOOUT}	LDOOUT(VOUT4) PIN Leakage			0.01	1	μA
R_{DIS_LDO}	LDOOUT(VOUT4) Output Discharge resistance			50		Ohm
Power Good OV/UV threshold						
PGOV	Vout1/2/3/4 Power Good Over Voltage Threshold, Rising			110		%
	Hysteresis			2.5		%
PGUV	Vout1/2/3/4 Power Good Under Voltage Threshold, Falling			90		%
	Hysteresis			2.5		%
Protection						
$V_{OUT,OVP}$	Vout1/2/3/4 Over Voltage Threshold, Rising		115	120	125	%
	Hysteresis			5		%
$V_{OUT,UVP}$	Vout1/2/3/4 Under Voltage Threshold, Falling		70	75	80	%
	Hysteresis			5		%
$V_{IN,OVP}$	VIN Over Voltage Threshold, Rising		19.5	21	22.5	V
	Hysteresis			1		V
T_{SD}	Thermal shutdown threshold, Rising			170		°C
	Hysteresis			20		°C

(1) Guaranteed by design and bench, not test in production.

TYPICAL CHARACTERISTICS

V_{IN}=10V, T_A=-40°C~125°C, unless otherwise noted.

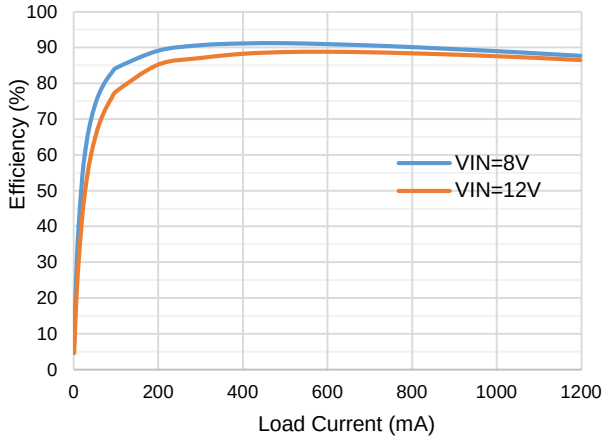


Figure 1. Buck1 Efficiency vs Load Current, V_{OUT1}=3.2V

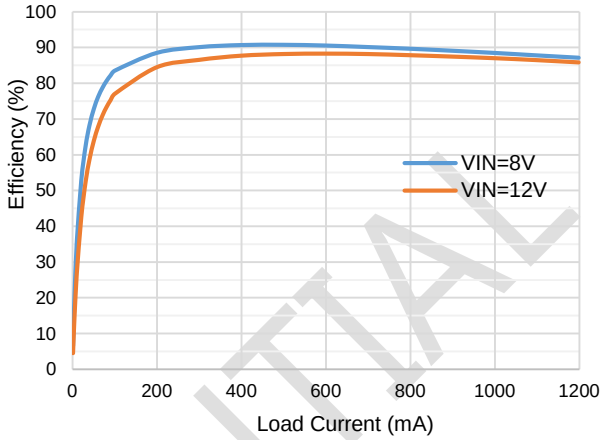


Figure 2. Buck1 Efficiency vs Load Current, V_{OUT1}=3.0V

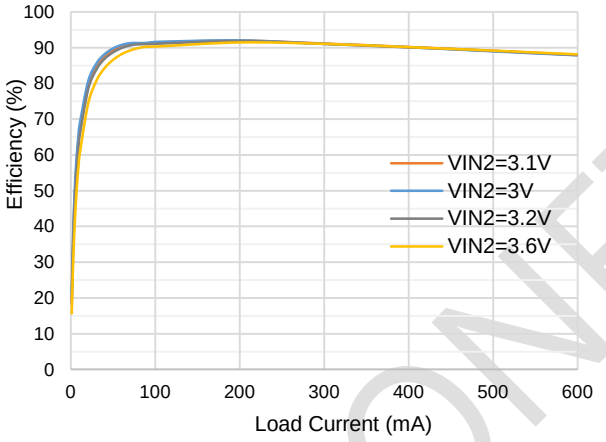


Figure 3. Buck2 Efficiency vs. Load Current, V_{OUT2}=1.8V

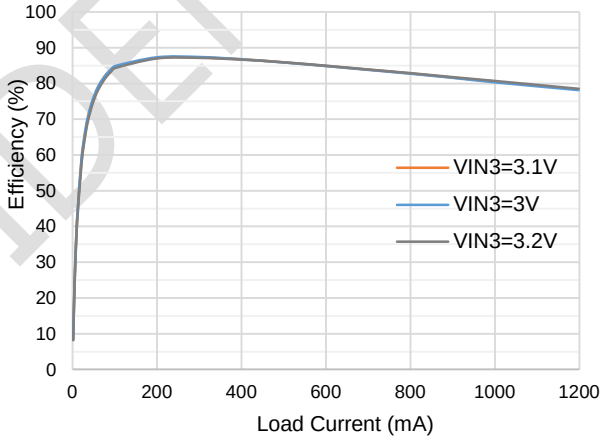


Figure 4. Buck3 Efficiency vs. Load Current, V_{OUT3}=1.2V

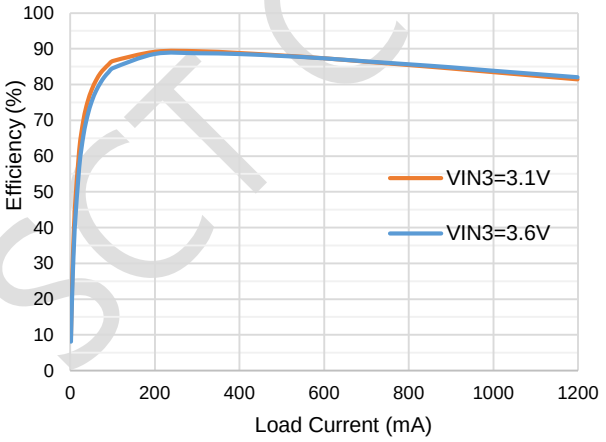


Figure 5. Buck3 Efficiency vs. Load Current, V_{OUT3}=1.5V

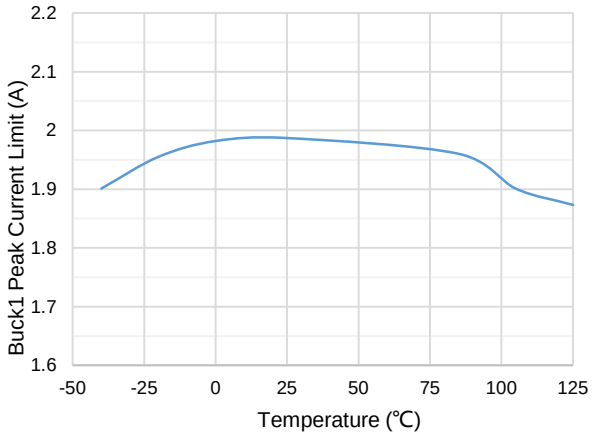


Figure 6. Buck1 Peak Current Limit vs. Temperature

TYPICAL CHARACTERISTICS (continued)

V_{IN}=10V, T_A=-40°C~125°C, unless otherwise noted.

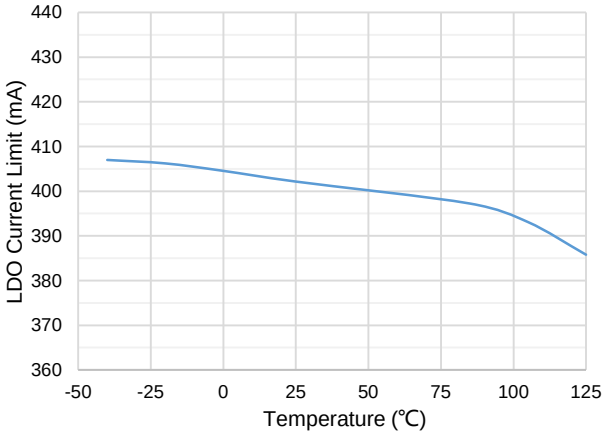


Figure 7. LDO Current Limit vs. Temperature

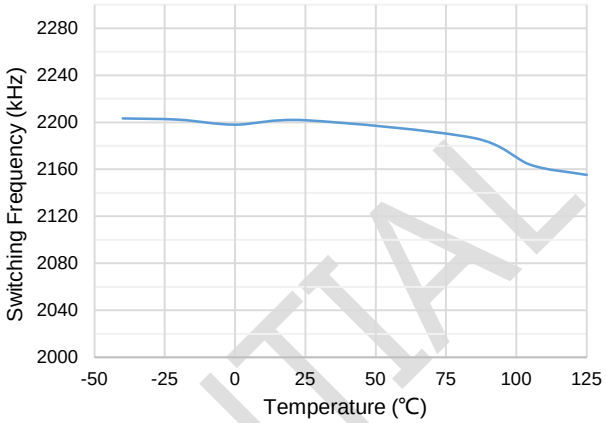


Figure 8. Switching Frequency vs. Temperature

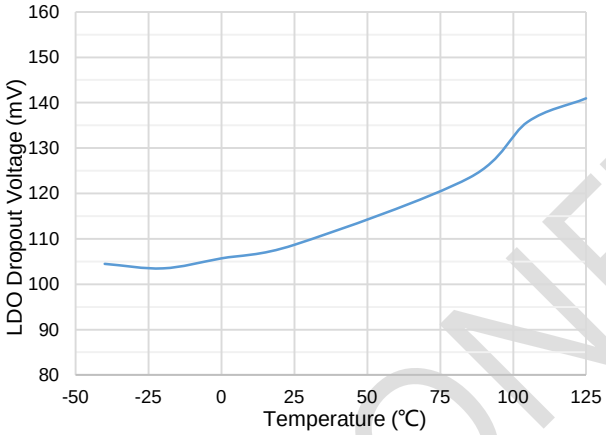


Figure 9. LDO Dropout Voltage vs. Temperature, ILDO=300mA

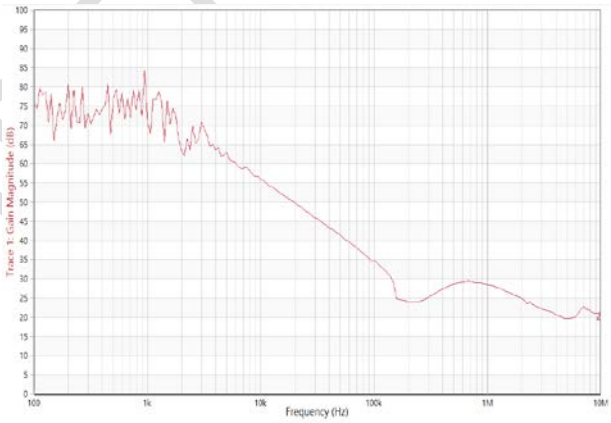


Figure 10. LDO PSRR, ILDO=100mA

FUNCTIONAL BLOCK DIAGRAM

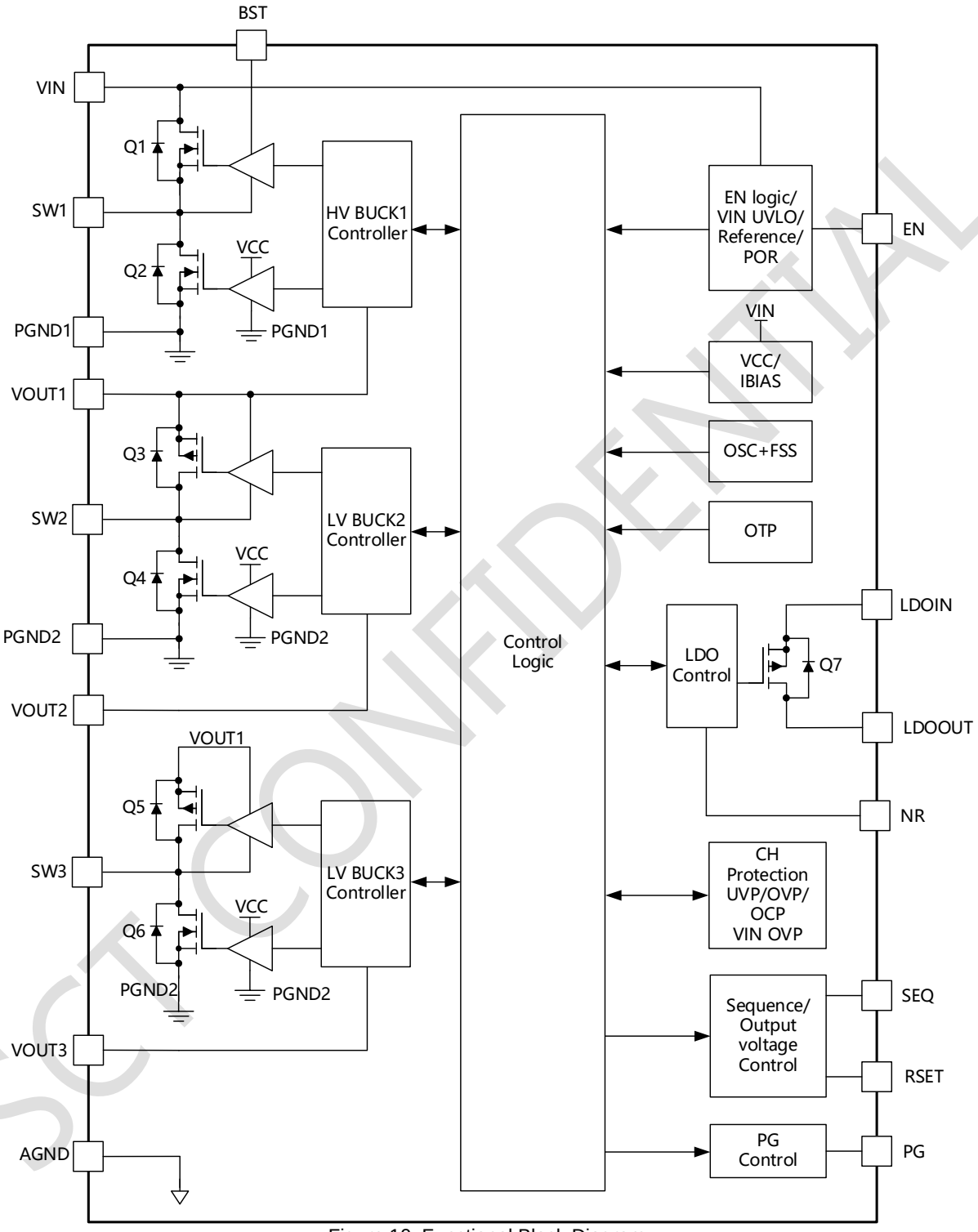


Figure 10. Functional Block Diagram

OPERATION

Overview

The SCT61240Q is a highly integrated power management IC (PMIC) optimized for automotive camera system. It integrates three high efficiency synchronous BUCK converters (HVBUCK1, LVBUCK2, LVBUCK3), and a high-PSRR low noise LDO with OV/UV monitoring on all outputs.

VOUT1 is the output of BUCK1, which is powered from VIN (Power Over Coax) and can output 1.2A continuous current with the output voltage set to LDOOUT+300mV/500mV or fixed 3.3V.

VOUT2 is the output of BUCK2, which is powered from VOUT1 and can output 600mA continuous current with the output voltage fixed to 1.8V.

VOUT3 is the output of BUCK3, which is powered from VOUT1 and can output 1.2A continuous current with the output voltage set to 1.1V/1.2V/1.3V/1.5V through RSET PIN for different sensors.

LDOOUT is the output of LDO, which is powered from VOUT1 (need to connect LDOIN to VOUT1) and can output 300mA continuous current with the output voltage set to 2.7V/2.8V/2.9V/3.3V through RSET PIN for different sensors.

With a compact QFN2.5x3.5 package, the SCT61240Q greatly reduces external components count and PCB space.

VIN and EN UVLO

When the VIN pin voltage rises above 3.8V and the EN pin voltage exceeds the enable threshold of 1.2V, the device is enabled. And the device disables when the VIN pin voltage falls below 3.8V or when the EN pin voltage is below 1.1V.

An internal 10MΩ resistor pulls EN pin to an internal 5V power supply allows the device to be enabled when EN pin is floating to simplify the system design.

High Efficiency Buck Converters

All the 3 BUCKs employ 2.2MHz fixed frequency peak current mode control with forced continuous conduction mode (FCCM). Built-in UVLO, soft-start (0.5ms/1ms/1.5ms/2ms options by OTP trim), compensation and hiccup (or latch off option by OTP trim) make the buck converters easily to be used by minimizing the off-chip component count.

For buck1, an external 100nF ceramic bootstrap capacitor between BST and SW1 pin powers high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The converters have proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

The converters implement over current protection with cycle-by-cycle limiting high-side MOSFET peak current and also low-side MOSFET valley current to avoid inductor current running away during unexpected overload and hiccup protection in output hard short condition. When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement even though the inductor current has already been clamped at over current limitation. Thus, output voltage drops below regulated voltage continuously. When output voltage loss regulation lasts for 100 us, the converter stops switching, after remaining OFF for 3.2 ms, the device will attempt to restart. The hiccup protection mode greatly reduces the average short circuit current to alleviate thermal issues and protect the regulator.

Over Voltage Protection

If an output exceeds the over voltage protection threshold, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again according to the SEQ and RSET setting. When entry hiccup, the output discharge will operate during the hiccup time.

Under Voltage Protection

If an output falls below the under voltage protection threshold, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again according to the SEQ and RSET setting. When entry hiccup, the output discharge will operate during the hiccup time.

Over Current Protection (OCP)

For the three bucks and LDO, the SCT61240Q provides both peak and valley current limit designed to limit the peak/valley inductor current to ensure that the switching currents remain within the device capabilities during overload conditions or during an output short circuit.

When the HS-FET turns on, the chip monitors the increased IL through the relevant operating main power switch. Once the peak IL exceeds the peak current limit threshold, the HS-FET turns off immediately, and the LS-FET turns on to conduct and decrease IL. The HS-FET does not turn on again until IL falls below the valley current limit threshold. If the feedback voltage makes EA's output level triggers the high clamp limit consecutively in a settled cycle, an over-current (OC) fault is reported and OCP is activated, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again according to the SEQ and RSET setting.

Power Good

The PG pin is a push-pull output. It goes to logic high when the device is powered on, and all outputs are within the power good range, and no faults reported. The high output level can be programmed to either 3.3V or 1.8V.

PG will assert low when any of below events occur:

- Buck1's output is out of power good range or VOUT OV/UV range or OCP
- Buck2's output is out of power good range or VOUT OV/UV range or OCP
- Buck3's output is out of power good range or VOUT OV/UV range or OCP
- LDO's output is out of power good range or VOUT OV/UV range or OCP
- Junction temperature is over Thermal Shutdown point
- VIN is higher than VIN OVP threshold

Hiccup or Latch off Protection

When below faults are detected, the SCT61240Q will enter hiccup or latch off mode (programmable option). When select hiccup mode and entry hiccup, all the channels shut off for 3.2ms, and then the normal power up sequence will start again according to the SEQ and RSET setting. When select latch off mode and entry latch off, all the channels shut off and not restart unless VIN/EN power on reset (POR).

The faults that make the device entry hiccup/latch off protection:

- Buck1's output is out of VOUT OV/UV range or OCP
- Buck2's output is out of VOUT OV/UV range or OCP
- Buck3's output is out of VOUT OV/UV range or OCP
- LDO's output is out of VOUT OV/UV range or OCP
- Junction temperature is over Thermal Shutdown point
- VIN is higher than VIN OVP threshold

Output Discharge

In order to discharge the energy of output capacitor during power off sequence, all channels have active discharge path from their output to ground. The discharge path is turn-on when channel is disabled.

Internal Soft-Start

The soft start function is implemented to prevent the PMIC output voltage from overshooting during start-up. When the PMIC starts up, the internal circuitry of each power rail generates a soft-start voltage that ramps up from 0V. The soft-start period lasts until the voltage on the soft-start capacitor exceeds the reference voltage. At this point, the reference voltage takes over.

Frequency Spread Spectrum

To meet CISPR and automotive EMI compliances, the SCT61240Q implements Frequency Spread Spectrum (FSS) function. The FSS circuitry shifts the 2.2MHz switching frequency within ±5% range and 1/512 of the switching frequency periodically. Therefore, the SCT61240Q can guarantee that the switching frequency does not drop into the 1.8MHz AM band limit.

Thermal Shutdown

The SCT61240Q protects the device from damage during excessive heat and power dissipation condition. Once the junction temperature exceeds 170C, the thermal sensing circuit disable all channels and enter hiccup or latch off. When the junction temperature falls below 150C and hiccup ends, then the device restarts.

Power on/off Sequence Control

For power on, the SCT61240Q supports 6 power-on sequences for buck2&3 and LDO through SEQ pin. Since the output of BUCK1 is the power for the next three channels, BUCK1 is always set to startup first.

For power off, through VIN/EN or entry hiccup/latch off, all channels power off simultaneously.

Connect a resistor between SEQ and GND to set the power on sequence before enabling the device. The SEQ detection only activated at the beginning of power on, and the sequence configuration is latched once SEQ detection done. When the resistance selected out of range, CH2&CH3&CH4 are disabled. Any change during the power on procedure is not guarantee to the correct power-on sequence.

Below table shows the power-on sequence with its corresponding resistance. CH1 is BUCK1, CH2 is BUCK2, CH3 is BUCK3, CH4 is LDO.

Table 1. Power-On Sequence Control

SEQ No.	SEQ Resistance(Ω)			Sequence			
	MIN	TYP	MAX				
SEQ1	0	0	3k	CH1	CH4	CH2	CH3
SEQ2	6k	8k	10k	CH1	CH2	CH4	CH3
SEQ3	14k	16k	18k	CH1	CH2	CH3	CH4
SEQ4	24k	27k	30k	CH1	CH3	CH2	CH4
SEQ5	40k	45.5k	50k	CH1	CH3	CH4	CH2
SEQ6	400k	Float	Float	CH1	CH4	CH3	CH2

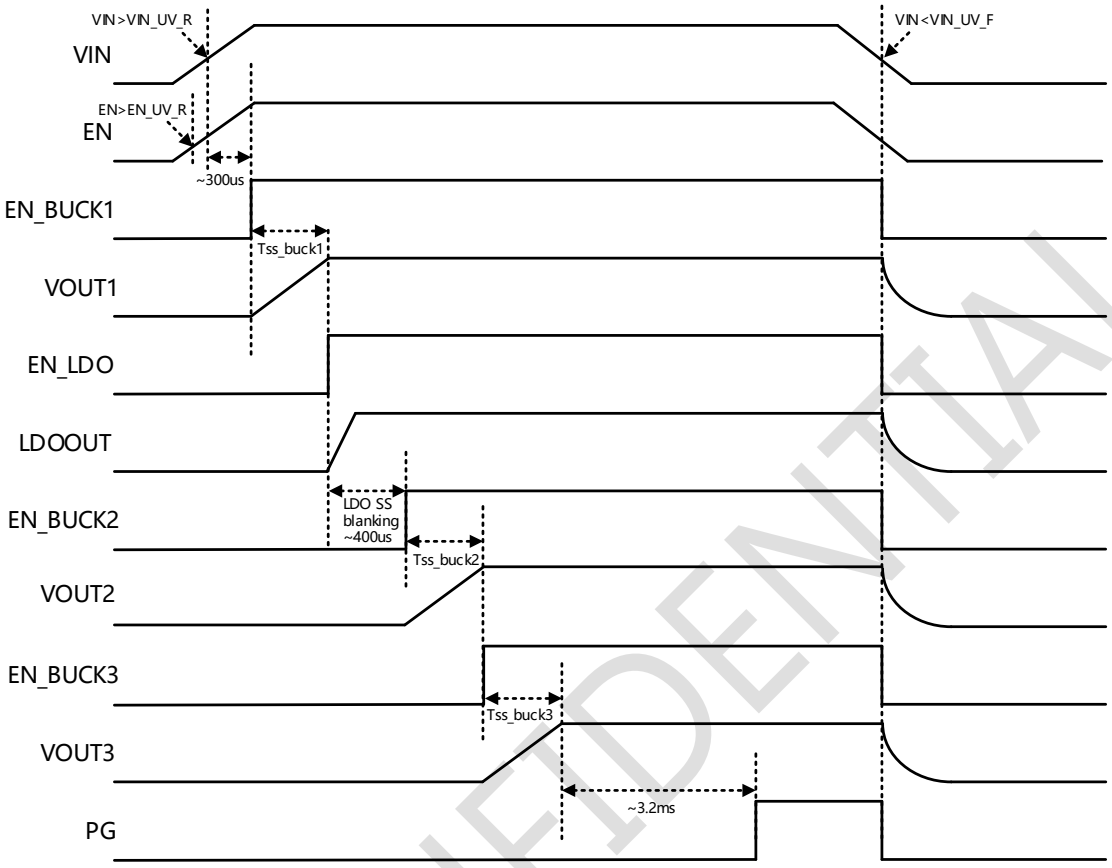


Figure 11. Example SEQ1 for SCT61240Q

Output Voltage Setting

The SCT61240Q provides 9 flexible voltage setting through RSET PIN for various sensors. Connect a resistor between RSET and GND to set the output voltage of each channel before enabling the device. The RSET detection only activated at the beginning of power on, and the output voltage configuration is latched once RSET detection done. Any change during the power on procedure is not guarantee to the correct output voltage setting.

Below table shows the output voltage setting with its corresponding resistance.

Table 2. Output Voltage Setting

RSET No.	RSET Resistance(Ω)			Output voltage(V)			
	MIN	TYP	MAX	BUCK1	BUCK2	BUCK3	LDO
VSET1	0	0	3k	3.1	1.8	1.2	2.8
VSET2	6k	8k	10k	3.0	1.8	1.2	2.7
VSET3	14k	16k	18k	3.1	1.8	1.1	2.8
VSET4	24k	27k	30k	3.1	1.8	1.5	2.8
VSET5	40k	45.5k	50k	3.2	1.8	1.2	2.9
VSET6	70k	76k	90k	3.6	1.8	1.1	3.3
VSET7	120k	127k	140k	3.6	1.8	1.3	3.3
VSET8	210k	230k	250k	3.6	1.8	1.5	3.3
VSET9	400k	Float	Float	3.2	1.8	1.1	2.9

APPLICATION INFORMATION

Typical Application

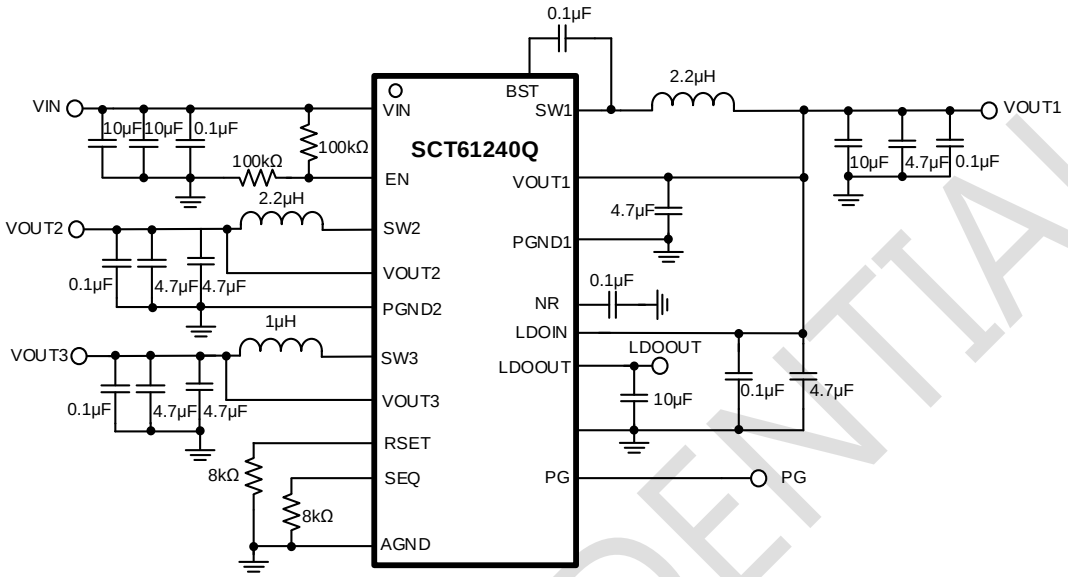


Figure 12. Application Schematic, 4V to 19V, PMIC Regulator at 2.2MHz

Design Parameters

Design Parameters	Example Value
Input Voltage	10V Normal 4V to 19V
Output Voltage	VOUT1: 3.0V VOUT2: 1.8V VOUT3: 1.2V LDOOUT: 2.7V
Maximum Output Current	VOUT1: 1.2A (in total) VOUT2: 0.6A VOUT3: 1.2A LDOOUT: 0.3A
Switching Frequency	2.2MHz
Output Voltage Ripple (peak to peak)	VOUT1: 10mV VOUT2: 2mV VOUT3: 4mV

Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set a higher input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. Use Equation 1 and Equation 2 to calculate the values of R_1 and R_2 resistors.

$$V_{rise} = \left(1 + \frac{R_1}{R_2}\right) * V_{ENrise} \quad (1)$$

$$V_{fall} = \left(1 + \frac{R_1}{R_2}\right) * V_{ENfall} \quad (2)$$

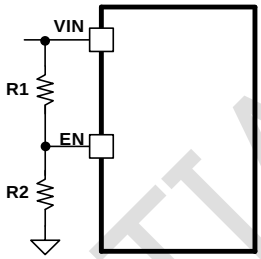


Figure 13. System UVLO by enable divide

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO
- V_{ENrise} is rising threshold of EN UVLO
- V_{ENfall} is falling threshold of EN UVLO

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 3.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (3)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 4 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (4)$$

Where

- L_{MIN} is the minimum inductance required
- f_{sw} is the switching frequency
- V_{OUT} is the output voltage

- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 5 and equation 6.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (5)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (6)$$

Where

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device. The most conservative approach is to choose an inductor with a saturation current rating greater than peak current limit. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT61240Q can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 7.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (7)$$

The worst case condition occurs at V_{IN}=2*V_{OUT}, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 9 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (9)$$

For this example, two 10μF, X7R ceramic capacitors rated for 50V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 10 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * {f_{SW}}^2 * L * C_{OUT} * V_{IN}} \quad (10)$$

Where

- ΔV_{OUT} is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 4.7μF ceramic output capacitors work for most applications. The LDO is specifically designed to work with a standard ceramic output capacitor to save space and improve performance. Larger output capacitors will improve load transient response and reduce noise at the cost of increased size. A 1μF to 20μF output capacitor should be placed to get stable output.

Application Waveforms

Vin=10V, RSET=SEQ=8kΩ, V_{OUT1}=3.0V, V_{OUT2}=1.8V, V_{OUT3}=1.2V, V_{OUT4}=2.7V,unless otherwise noted

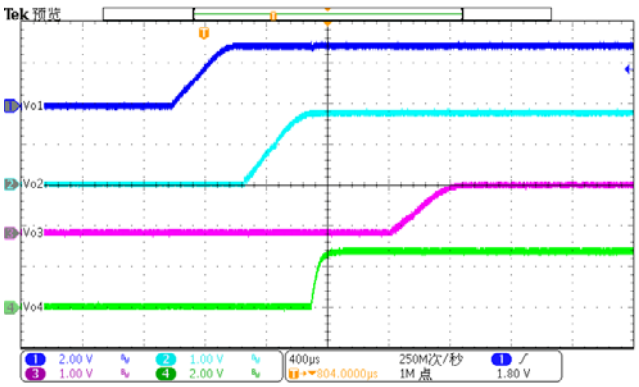


Figure 14. Power On (Io2=0.6A, Io3=1.2A, Io4=0.3A)

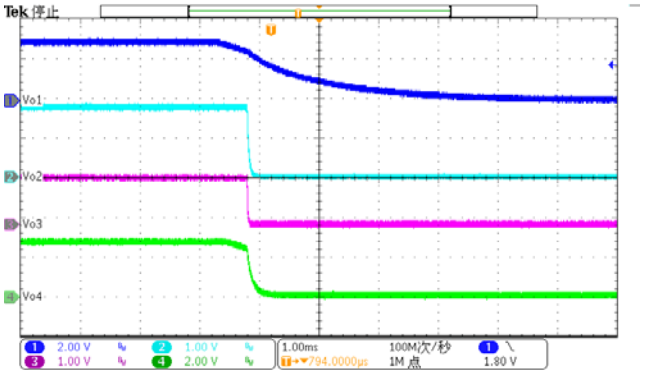


Figure 15. Power Off (Io2=0.6A, Io3=1.2A, Io4=0.3A)

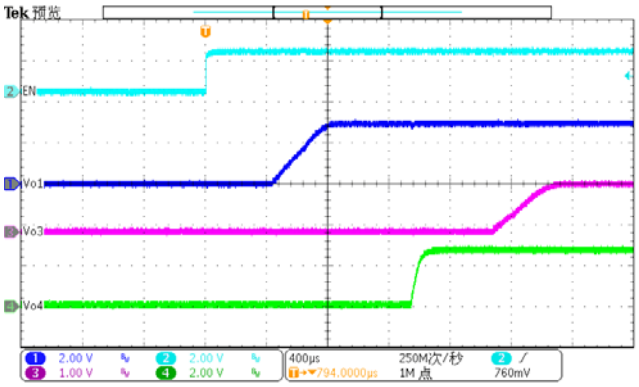


Figure 16. EN On (Io2=0.6A, Io3=1.2A, Io4=0.3A)

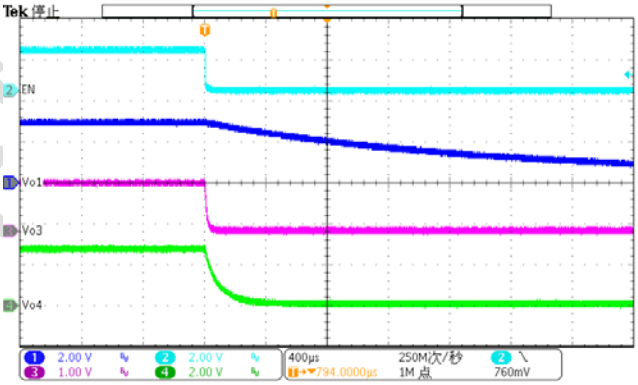


Figure 17. EN Off (Io2=0.6A, Io3=1.2A, Io4=0.3A)

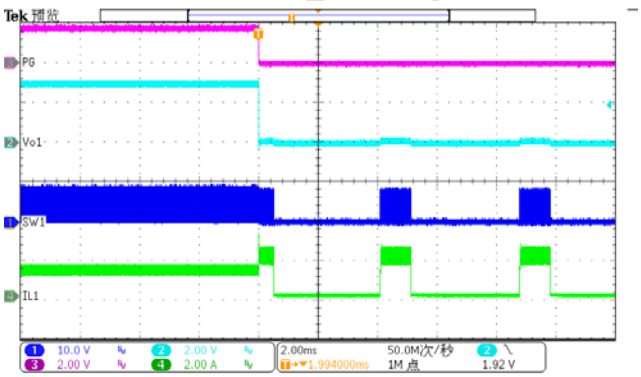


Figure 18. Buck1 Over Current Protection
(1.2A to hard short)

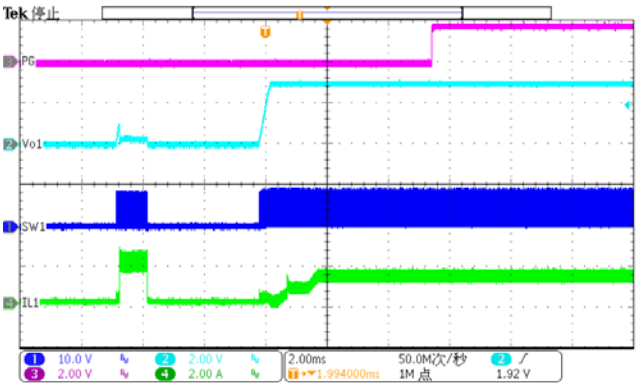


Figure 19. Buck1 Over Current Release
(hard short to 1.2A)

Application Waveforms (continued)

Vin=10V, RSET=SEQ=8kΩ, V_{OUT1}=3.0V, V_{OUT2}=1.8V, V_{OUT3}=1.2V, V_{OUT4}=2.7V,unless otherwise noted

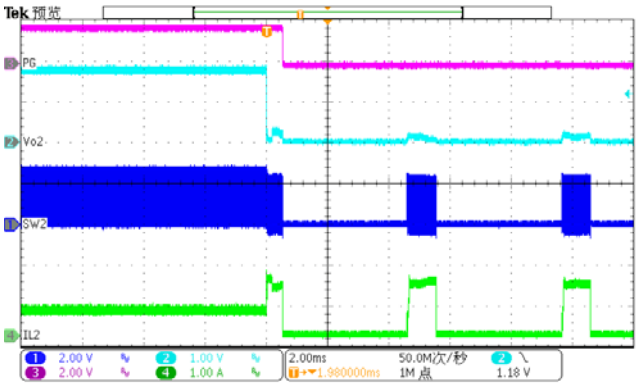


Figure 20. Buck2 Over Current Protection
(0.6A to hard short)

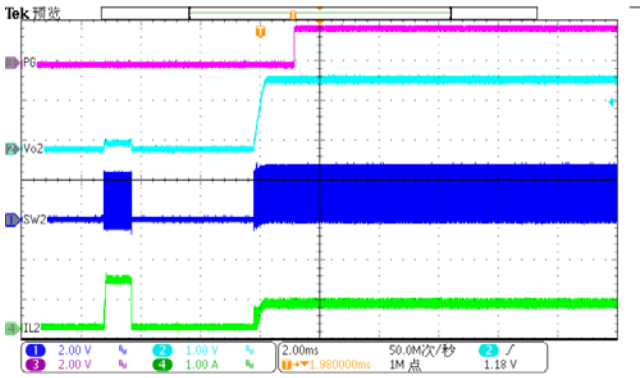


Figure 21. Buck2 Over Current Release
(hard short to 0.6A)

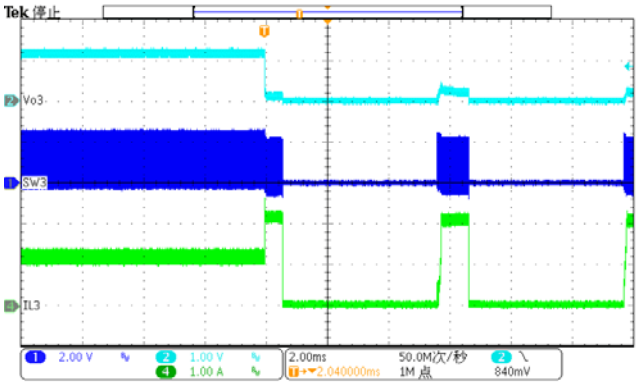


Figure 22. Buck3 Over Current Protection
(1.2A to hard short)

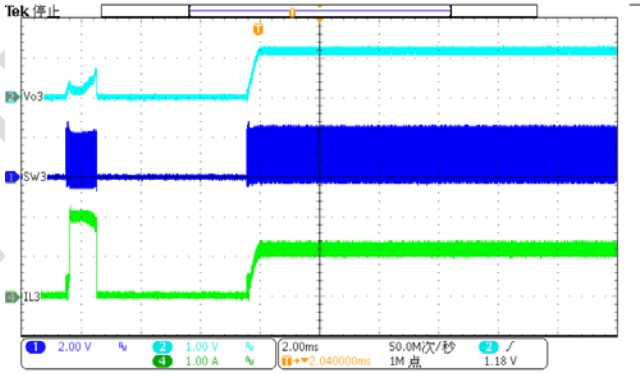


Figure 23. Buck3 Over Current Release
(hard short to 1.2A)

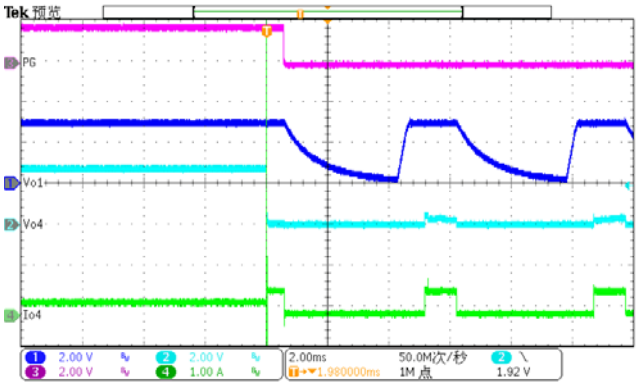


Figure 24. LDO Over Current Protection
(0.3A to hard short)

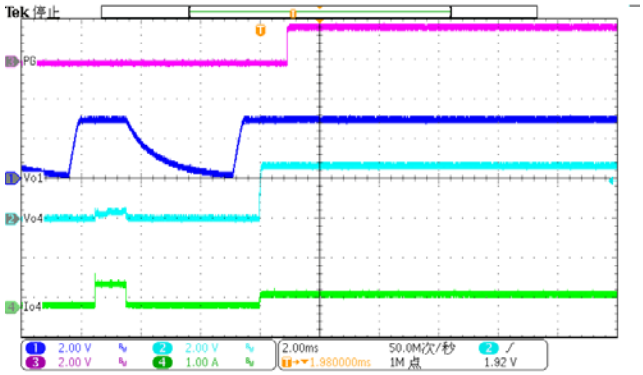


Figure 25. LDO Over Current Release
(hard short to 0.3A)

Application Waveforms (continued)

Vin=10V, RSET=SEQ=8kΩ, V_{OUT1}=3.0V, V_{OUT2}=1.8V, V_{OUT3}=1.2V, V_{OUT4}=2.7V,unless otherwise noted

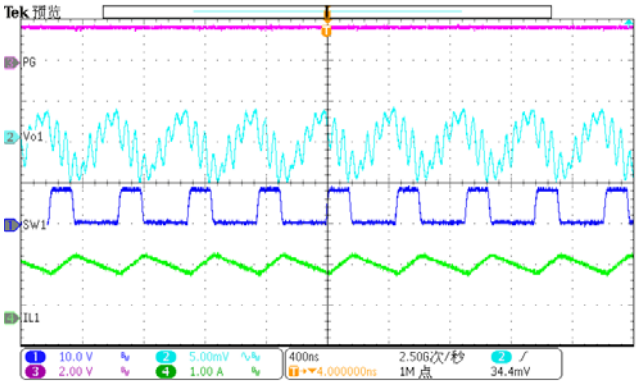


Figure 26. Buck1 Steady State (Io1 = 1.2A)

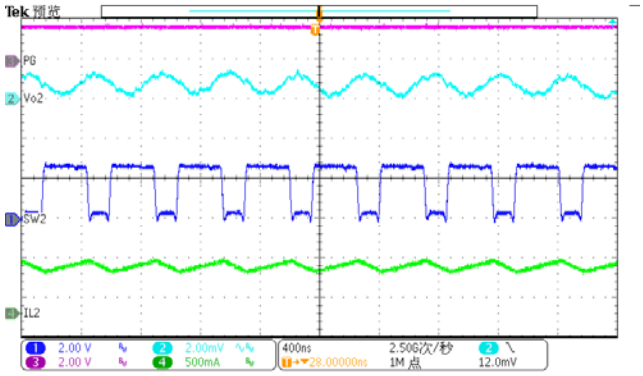


Figure 27. Buck2 Steady State (Io2 = 0.6A)

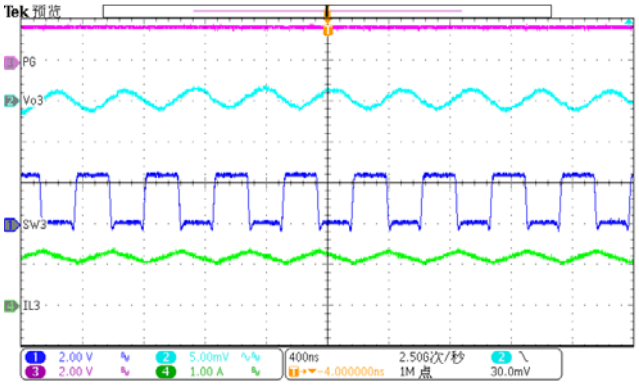


Figure 28. Buck3 Steady State (Io3 = 1.2A)

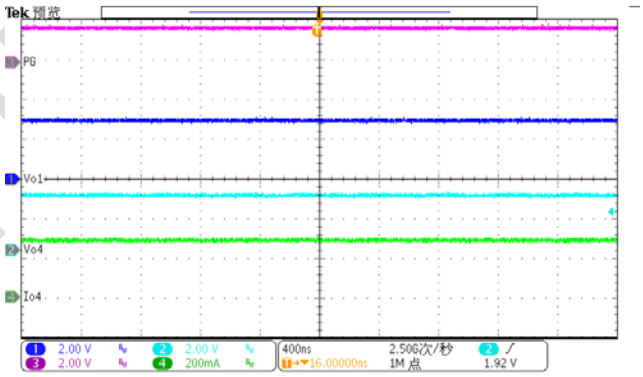


Figure 29. LDO Steady State (Io2 = 0.6A)

Layout Guideline

Proper PCB layout is a critical for SCT61240Q's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.
5. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. UVLO adjust resistors and feedback trace should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
7. For LDO low noise area, place an independent copper plane with AGND pin. Use this quiet AGND through LDO power path and sensitive pins NR, RSET, SEQ. To avoid noise interference, using vias to connect AGND to PGND with single point.
8. For achieving better thermal performance, a four-layer layout is strongly recommended.

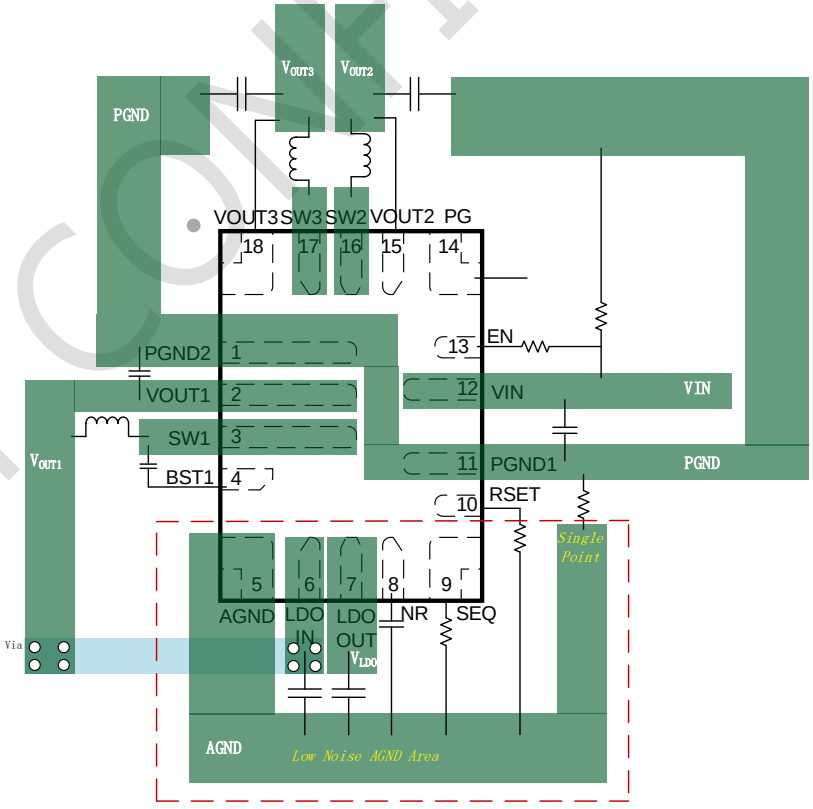
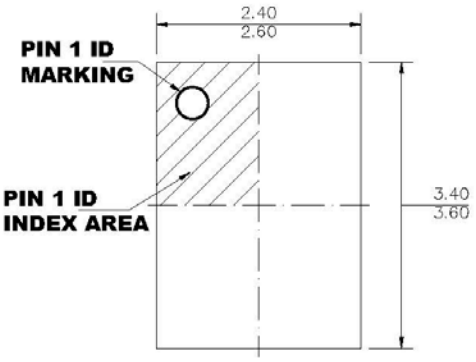
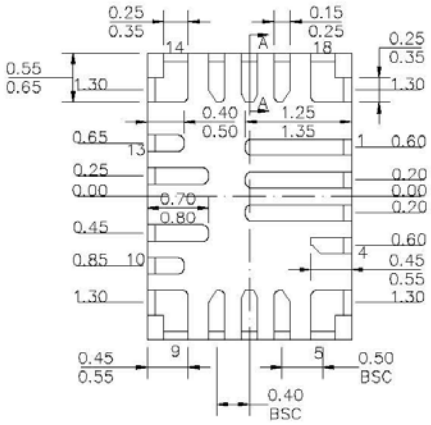


Figure 30. PCB Layout Example

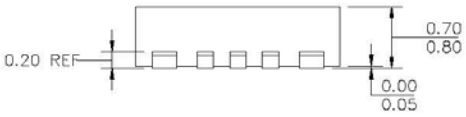
PACKAGE INFORMATION



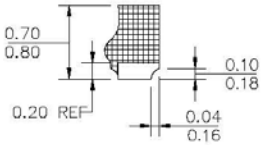
TOP VIEW



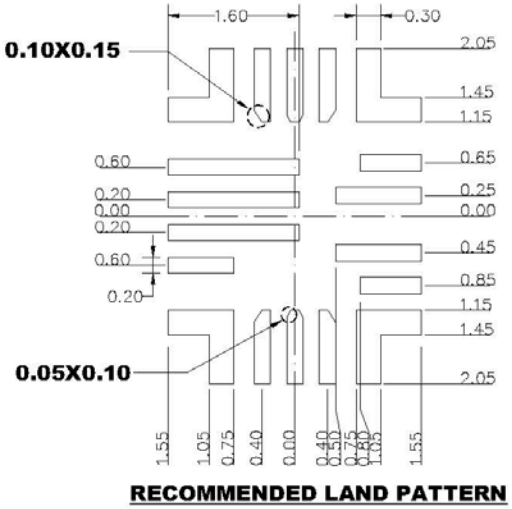
BOTTOM VIEW



SIDE VIEW



SECTION A-A



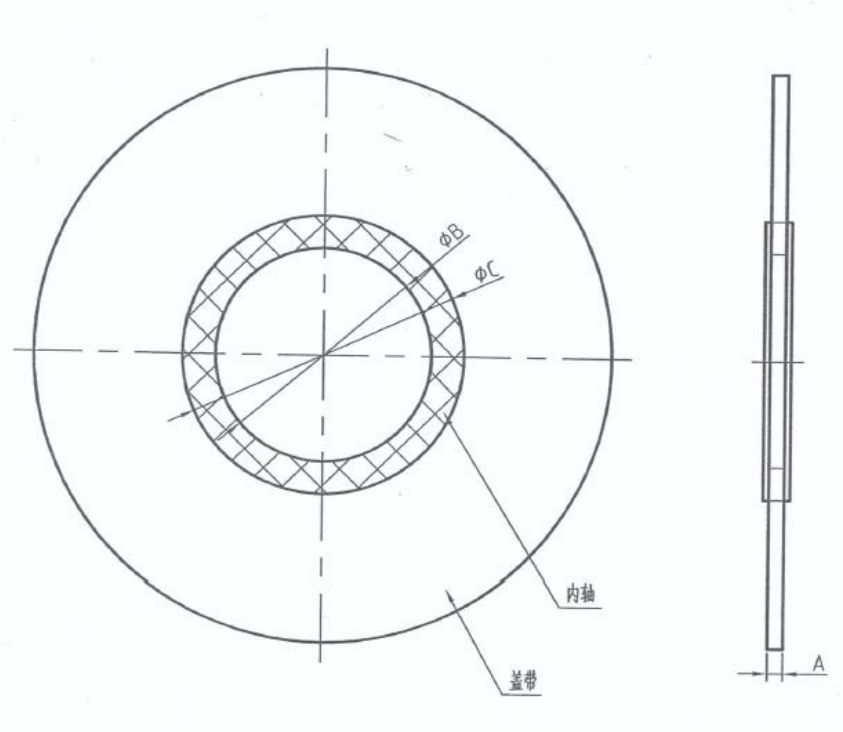
RECOMMENDED LAND PATTERN

NOTE:

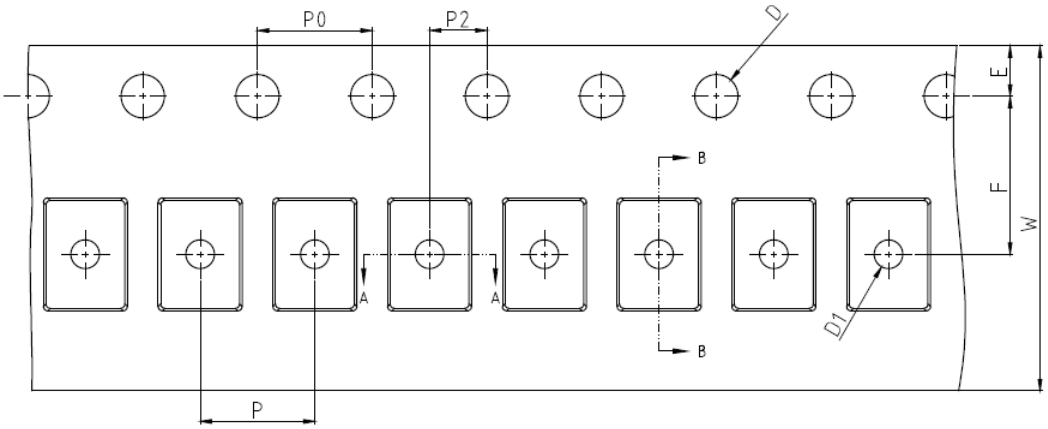
1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

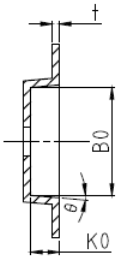
TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT61240Q Series	FCQFN	18	4000

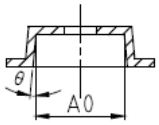


Type	$A_0^{+0.1}$ mm	Carrier Width	Diameter
PRA、F4DK	9.3	12	B=76.2±0.10mm C=92.2±0.25mm
HST	9.5	12	
HST	13.5	16	
HST、C800	21.3	24	
2420S	13.3	16	
2420S	21.3	24	
TIST300	9.9	12	





B-B



A-A

Symbol	Dimensions in Millimeters
A0	2.75±0.10
B0	3.75±0.10
D	$1.5^{+0.10}$
D1	1.00±0.10
E	1.75±0.10
F	5.50±0.05
K0	1.00±0.10
P	4.00±0.10
P0	4.00±0.10
P2	2.00±0.05
t	0.25±0.03
W	$12.00^{+0.30}_{-0.10}$
θ	5° max

